IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

AMERICAN PATENTS LLC, Plaintiff, v. MEDIATEK INC., ET AL., Defendants.	CIVIL ACTION NO. 6:18-cv-339-ADA **JURY TRIAL DEMANDED**

AMERICAN PATENTS' OPENING CLAIM CONSTRUCTION BRIEF

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EXHIBIT LIST

Exhibit No.	Exhibit Description
1	U.S. Patent No. 7,836,371
2	U.S. Patent No. 6,964,001
3	U.S. Patent No. 8,239,716
4	U.S. Patent No. 8,996,938
5	Excerpts from *The New Oxford American Dictionary* (1st ed. 2001) Oxford University Press
6	Excerpts from *IBM Dictionary of Computing* (10th ed. 1993) McGraw-Hill
7	Excerpts from *IEEE 100 The Authoritative Dictionary of IEEE Standards Terms* [7th ed. 2000] Standards Information Network, IEEE Press
8	Excerpts from *Microsoft Computer Dictionary* (5th ed. 2002) Microsoft Press
9	Excerpts from McGraw-Hill Dictionary of Electrical and Electronic Engineering (1984) McGraw-Hill
10	Excerpts from *IEEE Standard Glossary of Computer Hardware Terminology* (1995) The Institute of Electrical and Electronics Engineers, Inc.
11	Claim Construction order from *Intellectual Ventures I LLC v. Toshiba Corp.*, No. 13-cv-453-SLR, Dkt. 277 (D. Del. Dec. 17, 2015)

I. INTRODUCTION

Plaintiff American Patents submits its opening brief supporting its proposed claim constructions. American Patents accuses Defendants of infringing four patents: U.S. Patent Nos. 7,836,371 ("the '371 patent"); 6,964,001 ("the '001 patent"); 8,239,716 ("the '716 patent"); and 8,996,938 ("the '938 patent") (collectively, "the asserted patents" or "the '371 patent family"). The asserted patents, each titled "On-Chip Service Processor," are members of the same patent family and share a common specification.[1]

The parties agree on the proper construction of eight claim terms, and dispute the constructions of ten claim terms. But whereas Defendants' proposed constructions stray from the plain text of the claims, American Patents' proposals recognize that many of the claim terms have a plain and ordinary meaning readily understood by persons of ordinary skill in the art. Where Defendants seek to improperly write additional limitations into the claims, American Patents' proposals adhere to the claims as written, and as supported by the specification, prosecution history, and relevant extrinsic evidence. The Court should thus adopt American Patents' proposed constructions and reject Defendants' proposed constructions.

II. TECHNOLOGY BACKGROUND

The '371 patent family is directed to integrated circuits ("ICs") that include on-chip circuits for test and debug operations. At the time of the invention, technology for building integrated circuits had advanced to allow for more and more digital systems, or parts of digital systems, to be integrated into a single component. Existing testing and debugging solutions were unsatisfactory for use with these increasingly complex ICs. Prior art solutions included the use of external probes to monitor the IC, but these did not reliably and precisely capture signals. Other approaches, such as the use of so-called "shadow registers," did not allow sufficient visibility into the inner workings of the chip and were expensive to implement on a large scale.

[1] For simplicity, unless otherwise noted, all "xx:yy" citations are to the specification of the '371 patent.

The '371 patent family addresses these issues by disclosing special on-chip circuits, which are used to observe the internal workings of an IC. As compared to prior art test and debug methodologies, the circuits of the '371 patent family may operate at internal IC clock rates; allow for access to, and selection of, more internal points in the system; reduce the amount of test logic that might have been required elsewhere on the chip; and improve the accuracy of observations.

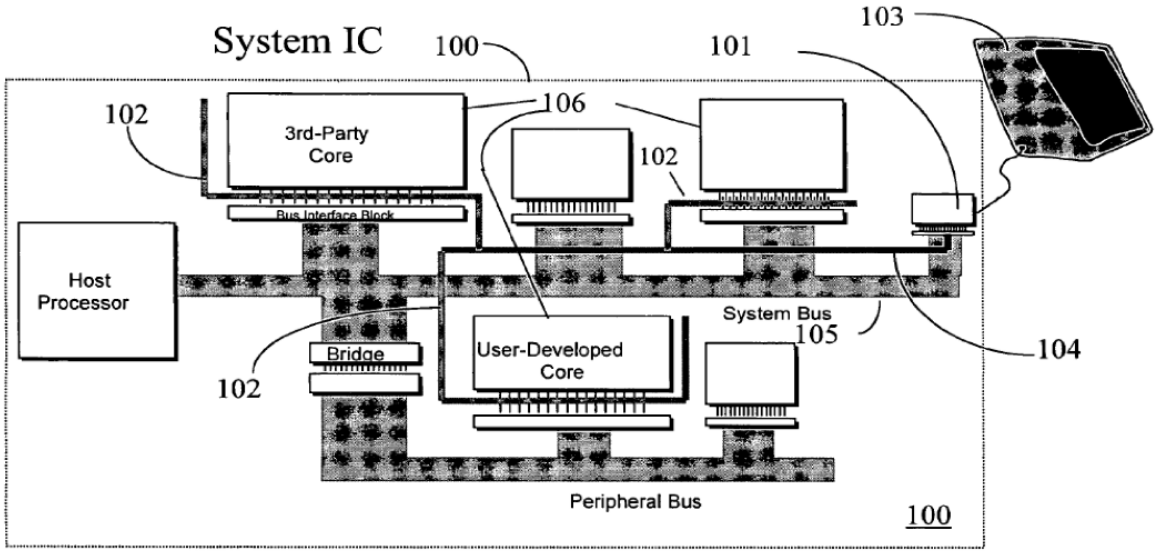

Figure 1b

Figure 1b shows an exemplary embodiment of the invention. This high-level diagram shows a complex IC 100 having various logic blocks 106. Figure 1b shows the IC with a service processor unit ("SPU") 101, which is coupled to the IC system bus 105 and an added test bus 104. The test bus 104 is connected to test wrappers 102, which provide communication channels into selected blocks 106. The SPU 101 provides a connection to an external diagnostics console 103 to view and test the internal workings of the IC. *See* 6:23-32.

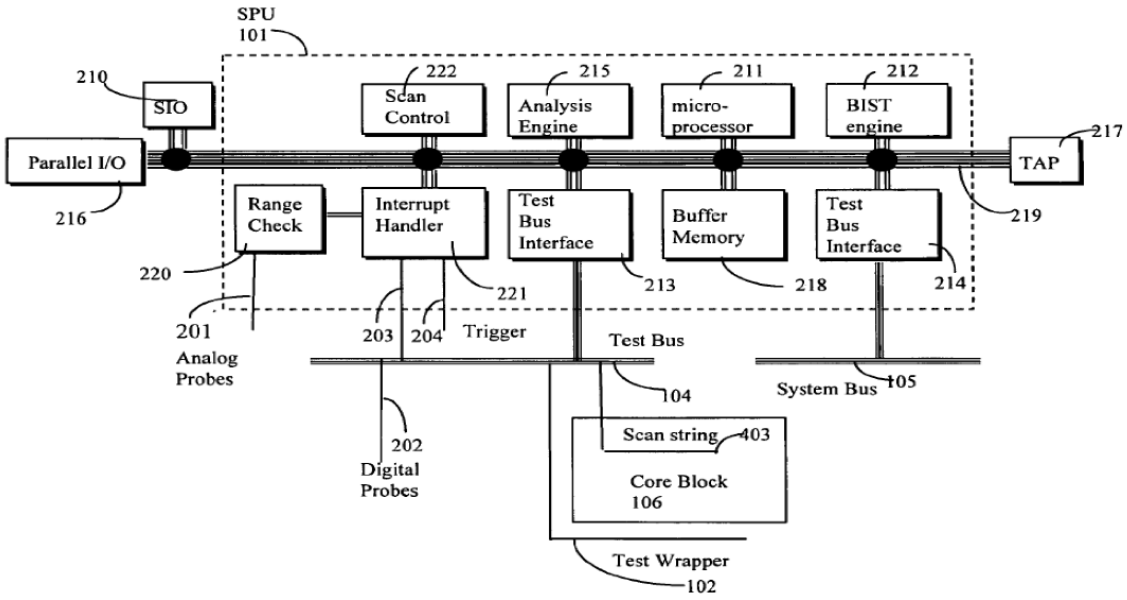

Figure 2

Figure 2 shows the exemplary SPU of Fig. 1 in greater detail, including several extended function units ("EFUs"), such as a control unit (e.g., a microprocessor 211), a buffer memory unit 218, and an analysis engine 215, all interconnected by a processor bus 219. *See* 6:33-41. The processor bus 219 is also connected to a serial input/output interface (SIO) 210, a parallel input/output interface (PIO) 216, and a test access port (TAP) 217, to provide communication between the SPU 101 and the external world. *See* 6:42-49. Interrupt handler 221 receives signals gathered from analog probe lines 201, trigger event lines 204, or test bus 104. The interrupt handler 221 passes captured values to the analysis engine 215. *See* 6:50-65. The analysis engine 215 has trigger logic which may stop the analysis engine from capturing new data when a trigger is detected, or, in a different embodiment, may cause the analysis engine to capture new data only when a trigger is received. *See* 10:64-11:2, 11:55-59. These are just some of the embodiments and examples described in the patents' specification.

Claim 7 is illustrative of the claimed subject matter of the '371 patent:

7. An integrated circuit comprising:

one or more logic blocks to generate one or more system-operation signals at one or more system-operation clock rates;

a system bus; and

a service processor unit, said service processor unit comprising:

a control unit;

a buffer memory; and

a system bus interface,

wherein said service processor unit is adapted to perform capture and analysis of system operation signals on said system bus during normal system operation through said system bus interface.

Claim 5 is illustrative of the claimed subject matter of the '001 patent:

5. An integrated circuit comprising:

a multiplicity of logic blocks:

an on-chip logic analyzer with a multiplicity of input ports: and

a multiplicity of probe lines:

wherein each of said probe lines is adapted to capture signals from said logic blocks and to propagate said signals to one of said multiplicity of input ports of said on-chip logic analyzer, said input ports of said on-chip logic analyzer comprising:

means to capture said signals from said probe lines:

means to align said signals propagated through said probe lines to create aligned signals: and

means to capture said aligned signals.

Claim 1 is illustrative of the claimed subject matter of the '716 patent:

1. An integrated circuit comprising:

one or more logic blocks configured to generate one or more system operation signals at one or more system operation clock rates;

a service processor unit configured to perform one or more debug operations on one or more of said logic blocks, the service processor unit comprising:

a control unit,

a buffer memory,

an analysis engine, and

a bus interface; and

a multiplicity of probe lines configured to capture and propagate one or more of said one or more system operation signals from said logic blocks to said service processor unit during normal system operation;

wherein said analysis engine is configured to align signals received from said probe lines during normal system operation.

Claim 1 is illustrative of the claimed subject matter of the '938 patent:

1. An integrated circuit comprising:

one or more logic blocks configured to generate one or more system operation signals at one or more system operation clock rates;

a service processor unit configured to perform one or more debug operations on one or more of the logic blocks, the service processor unit comprising:

a control unit configured to control the service processor unit;

a memory;

an analysis engine; and

a bus interface; and

a multiplicity of probe lines configured to capture and propagate one or more of the one or more system operation signals from the logic blocks to the service processor unit.

III. LEGAL STANDARDS

Claim construction begins with the claims, and "the context in which a term is used in the asserted claim can be highly instructive." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc). Courts must read claims "'in view of the specification, of which they are a part.'" *Id.* at 1315 (quoting *Markman*, 52 F.3d at 979). The Court may also look to the prosecution history and, "less significant[ly]," to extrinsic evidence such as technical treatises and dictionaries in construing the claims. *Id.* at 1317 (internal quotations omitted).

The "words of a claim 'are generally given their ordinary and customary meaning.'" *Id.* at 1312 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *see also Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time." (internal quotations omitted)) (vacated on other grounds). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date

of the patent application." *Phillips*, 415 F.3d at 1313. "Giving a term its plain and ordinary meaning does not leave the term devoid of any meaning whatsoever. Instead, 'the "ordinary meaning" of a claim term is its meaning to the ordinary artisan after reading the entire patent.'" *Match Group, LLC v. Bumble Trading Inc.*, No. 6:18-cv-80-ADA, Dkt. 107, at 1 (W.D. Tex. Aug. 15, 2019) (quoting *Phillips*, 415 F.3d at 1321).

"Although the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims." *Comark Comm'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (internal quotations omitted). "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

Indeed, "[t]he 'only two exceptions to [the] general rule' that claim terms are construed according to their plain and ordinary meaning are when the patentee (1) acts as his/her own lexicographer or (2) disavows the full scope of the claim term either in the specification or during prosecution." *True Chem. Solns., LLC v. Performance Chem. Co.*, No. 7:18-cv-78-ADA, Dkt. 64, at 3 (W.D. Tex. Sept. 25, 2019) (quoting *Thorner v. Sony Comp. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)). To act as his/her own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term," and "clearly express an intent to define the term." *Thorner*, 669 F.3d at 1365. To disavow the full scope of a claim term, the patentee's statements in the specification or prosecution history must represent "a clear disavowal of claim scope." *Id.* at 1366. Thus, when "an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

IV. AGREED CLAIM TERMS

The parties agree on the constructions of the following claim terms:

No.	Claim Term(s), Phrase(s), or Clause(s)	Agreed Construction
1	analysis (Claims 1-2, 7 of the '371 patent)	detection of events or states
2	analysis engine (Claims 1-3 of the '716 patent; Claims 1-4, 22 of the '938 patent)	a component that captures signals for analysis
3	[perform] capture [configured / adapted to] capture (Claim 5 of the '001 patent; Claims 1-2, 7 of the '371 patent; Claim 1 of the '716 patent; Claims 1, 22 of the '938 patent)	acquisition of data in a form that is capable of storage acquire data in a form that is capable of storage
4	logic analyzer (Claims 15-16 of the '938 patent)	a component that captures signals for analysis
5	on-chip logic analyzer (Claims 5-6 of the '001 patent)	a component that captures signals for analysis
6	service processor unit (Claims 1-2, 7-10 of the '371 patent; Claim 1 of the '716 patent; Claims 1, 5-7, 10, 22 of the '938 patent)	a unit containing a processor that performs test and debug operations
7	system bus (Claim 7 of the '371 patent)	a communication path within a system that can be shared
8	system operation signals (Claims 1-2, 7 of the '371 patent; Claim 1 of the '716 patent; Claims 1, 10-11, 15, 22 of the '938 patent)	signals internal to the integrated circuit

V. DISPUTED CLAIM TERMS (NON-MEANS-PLUS-FUNCTION)

A. "An integrated circuit comprising:"

No.	Term	American's Proposed Construction	Defendants' Proposed Construction
1	An integrated circuit comprising: (All asserted independent claims)	The preambles are limiting.	The preambles are not limiting.

The parties dispute whether the common preamble of the asserted claims is limiting. "In general, a preamble limits the invention if it recites essential structure or steps, or if it is necessary to give life, meaning, and vitality to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (internal quotations omitted). Here, the common preamble both provides an antecedent basis for further claim limitations and is needed to give structure and meaning to the claims.

As an initial matter, each member of the '371 patent family is titled "On-Chip Service Processor," indicating that being "on-chip" is a key feature of the invention. To those of ordinary skill in the art, "chip" is synonymous with "integrated circuit," and "on-chip" means "denoting or relating to circuitry included in a single integrated circuit . . . ." Ex. 5 [New Oxford Am. Dict.] at 1195; *see also* Ex. 10 [IEEE Std. Glossary of Comp. Hardware Terminology] at 16 ("chip. (1) *See:* integrated circuit."), 48 ("integrated circuit (IC). . . . *Syn:* chip."); Ex. 8 [Microsoft Comp. Dict. 5th Ed.] at 98 ("chip. *n. See* integrated circuit."); Ex. 6 [IBM Dict. of Computing] at 102 ("chip (1) Synonym for integrated circuit (IC)."), 347 ("integrated circuit (IC) . . . Synonymous with microchip, chip."). So, fundamentally, the invention is directed to components which are part of a chip, or IC.

The preamble, which recites "[a]n integrated circuit comprising" various components, echoes this key feature and is essential to give structure and meaning to the claims. The focus of the '371 patent family is on-chip solutions for the test and diagnosis of problems ***in an integrated circuit***. *See* 1:24-27. The patents recognize the problem of increasingly complex ICs

and the need for testing solutions that are precise, reliable, and cost-effective. *See supra*. The '371 family of patents addresses this problem by disclosing SPUs which are incorporated within an integrated circuit—not external systems like those employed in the prior art. *See* 1:57-63, 2:47-49, 2:54-57, 4:33-34 ("In accordance with the present invention, a Service Processor Unit (SPU) is incorporated within an integrated circuit."). As a result, the nature of the disclosed test and debug infrastructure as ***part of*** the integrated circuit is essential to give "life, meaning, and vitality" to the claims, and helps to distinguish the invention from the prior art.

Further, the preamble provides antecedent basis for the "integrated circuit" as claimed in certain of the dependent claims. *See, e.g.*, '371 patent, cls. 6 ("The integrated circuit according to claim 1, wherein said service processor unit is adapted to monitor ***said integrated circuit***."), 9 ("The integrated circuit according to claim 7, wherein said service processor unit is adapted to perform debug operations of ***said integrated circuit***."), 10 ("The integrated circuit according to claim 7, wherein said service processor unit is adapted to monitor ***said integrated circuit***.") (emphases added); '001 patent, cl. 6. "[D]ependence on a particular disputed preamble phrase for antecedent basis may limit claim scope because it indicates a reliance on both the preamble and claim body to define the claimed invention." *Catalina Mktg.*, 289 F.3d at 808, *citing Bell Comm'ns Rsh., Inc. v. Vitalink Comm'ns Corp.*, 55 F.3d 516, 620 (Fed. Cir. 1995). Because "the claim drafter cho[se] to use *both* the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." *Bell Comm'ns Rsh.*, 55 F.3d at 620 (emphasis in original).

B. "align signals" / "align . . . signals" / "aligned signals"

No.	Term	American's Proposed Construction	Defendants' Proposed Construction
2	align signals / align . . . signals aligned signals	Plain and ordinary meaning	correct path delay differences between the probe points of the multiplicity of probe lines signals that result from

	(Claims 5, 6 of the '001 patent; Claims 1, 3 of the '716 patent; Claims 2, 4, 15, 22 of the '938 patent)		being aligned [see "align signals" construction]

The parties dispute whether this term requires construction. The Court should construe this term to have its plain and ordinary meaning.

Both laypersons and persons skilled in the art would readily understand the meaning of the phrase "align[ed] signals" without further construction. For instance, to "align" means to "put (things) into correct or appropriate relative positions." Ex. 5 [New Oxford Am. Dict.] at 40; *see also* Ex. 9 [McGraw-Hill Dict. Of Elec. Eng.] at 23 (defining "alignment": "The process of adjusting components of a system for proper interrelationship, including the adjustment of tuned circuits for proper frequency response and the time synchronization of the components of a system."). And as Defendants' own proposed construction for "aligned signals" shows, the word "signals" does not itself require construction.

The specification uses this claim phrase consistently with its plain and ordinary meaning. As discussed in the specification, alignment of signals occurs via components of the analysis engine or logic analyzer, which select between incoming signals to "compensate[] for the path delay differences among the different probe points by realigning capture times of signals captured in the analysis engine 215." 10:61-63; *see generally* 10:22-64, Figs. 9a & 9b. In another embodiment, probe storage elements ("PSEs") 1000, comprising channels of the logic analyzer, are used "to align the data with respect to one another." 12:51-52; 13:2-4; *see generally* 13:1-17. Because the patents use this claim phrase consistently with the understanding of persons of ordinary skill in the art, the Court should afford it its plain and ordinary meaning. *See Match Group, LLC*, No. 6:18-cv-80-ADA, Dkt. 107, at 1 ("[T]he 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent.").

The Court should also reject Defendants' proposed construction because it is overly limiting. Defendants cannot show that patentees acted as their own lexicographer or disavowed the full scope of this claim term either in the specification or during prosecution. Had the

patentees wished to incorporate the limiting language that Defendants propose into the claims, they could have done so. Defendants' proposal also introduces limitations that are without antecedent basis in the claims—namely, "the probe points"—that risk confusing the jury. In sum, Defendants seek to import this limitation from the specification, but lack grounds for doing so. *See, e.g.*, *Comark Comm'ns, Inc.*, 156 F.3d at 1187 ("[T]he term 'video delay circuit' has a clear and well-defined meaning," and "is not so amorphous that one of skill in the art can only reconcile the claim language with the inventor's disclosure by recourse to the specification.").

C. "debug operations"

No.	Term	American's Proposed Construction	Defendants' Proposed Construction
3	debug operations (Claim 9 of the '371 patent; Claim 1 of the '716 patent; Claims 1, 22 of the '938 patent)	Plain and ordinary meaning *Alternatively:* diagnostic operations	operations that identify errors in captured signals

The parties primarily dispute whether the word "debug" in this claim term requires construction. The Court should give this term its plain and ordinary meaning. "Debug" is a term familiar to both laypersons and those of ordinary skill in the art. *See, e.g.*, Ex. 6 [IBM Dict. of Computing] at 180 (defining "debug," in part, as: "To detect, diagnose, and eliminate errors in programs."); Ex. 5 [New Oxford Am. Dict.] at 470 (defining "debug" as: "identify and remove errors from (computer hardware or software)"). So the term "debug operations" needs no construction.

If the Court concludes, however, that construction of this term would help the jury, the appropriate construction is "diagnostic operations." Persons of ordinary skill in the art understand "debugging" to be synonymous with "diagnosis." *See, e.g.*, Ex. 6 [IBM Dict. of Computing] at 180 (defining "debug," in part, as: "To detect, diagnose, and eliminate errors in programs."); Ex. 5 [New Oxford Am. Dict.] at 470 (defining "diagnostic": "a program or routine that helps a user to identify errors"). This is further borne out by the specification, which uses

the two terms interchangeably. *See* 1:24-27 ("The present invention is related to the ***testing and debugging*** of electronic systems, and, in particular, to on-chip circuits for the ***test and diagnosis*** of problems in an integrated circuit." (emphasis added)).

The specification also describes a range of activities in connection with test and debug operations, all of which are consistent with the normal meaning of test and debug or diagnostic operations. For instance, the Abstract describes "observ[ing] states" in user-definable logic and circuits; "provid[ing] pseudo-random bit sequences to user-definable logic"; and "capturing sequences of logic states." The specification also describes verifying ***correct*** system behavior in addition to erroneous behavior. *See* 1:32-35 ("The captured signals can then be examined to verify correct system behavior or, alternatively, to identify the time and the nature of erroneous behavior in the system."); *see also* 4:49-62 (describing test and debug features). These activities are consistent with the types of debug operations described in technical dictionaries and thus are consistent with the plain and ordinary meaning of this claim term. *See, e.g.*, Ex. 7 [IEEE 100 The Authoritative Dict. of IEEE Stds. Terms 7th Ed.] at 277 (defining "debug": "(1) To examine or test a procedure, routine, or equipment for the purpose of detecting and correcting errors."); Ex. 8 [Microsoft Comp. Dict.] at 148 (defining "debug," in part: "To detect, locate, and correct logical or syntactical errors in a program or malfunctions in hardware."); Ex. 6 [IBM Dict. of Computing] at 181 (defining "debugging mode": "A mode in which a program provides detailed output about its activities in order to aid a user in detecting and correcting errors in the program itself or in the configuration of the program or system."); *see also* Ex. 5 [New Oxford Am. Dict.] at 439 (defining "debug": "identify and remove errors from (computer hardware or software)").

In contrast, Defendants' proposed construction is improperly narrow and without support in the specification. Neither the plain and ordinary meaning, nor the specification's description of test and debug operations, is narrowly cabined to "identify[ing] errors"; nor is it limited to "captured signals." *See supra*. Defendants' narrow construction may improperly exclude certain features of debug operations.

D. "during normal system operation"

No.	Term	American's Proposed Construction	Defendants' Proposed Construction
4	during normal system operation (Claims 1-2, 7 of the '371 patent; Claim 1 of the '716 patent)	Plain and ordinary meaning American agrees that the plain and ordinary meaning of "during normal system operation" may include test and debug operations.	Plain and ordinary meaning Defendants add the following note: The plain and ordinary meaning of "during normal system operation" includes operations under test constraints or in a test mode.

The parties agree that this term bears its plain and ordinary meaning. This phrase simply indicates a period during which the system is operating normally; it requires no construction or technical definition beyond that plain meaning.

In a prior litigation involving the '371 patent, the U.S. District Court for the District of Delaware agreed, construing the phrase "system operation signals during normal system operation" to mean "signals internal to the integrated circuit when the integrated circuit is operating normally." Ex. 11 [*Intellectual Ventures I LLC v. Toshiba Corp.*, No. 13-cv-453-SLR, Dkt. 277, (D. Del. Dec. 17, 2015)] at 15-16. The Court need do nothing more than reconfirm this plain and ordinary meaning—whether or not by explicit claim construction—and reject Defendant's proposal to alter the term's meaning in the guise of clarification. *See, e.g., ActiveVideo Networks, Inc. v. Verizon Comm'ns, Inc.*, 694 F.3d 1312, 1325-26 (Fed. Cir. 2012) (holding that by rejecting accused infringer's proposed construction of a claim term and giving the term its plain and ordinary meaning, the district court sufficiently resolved the claim construction dispute).

That said, American Patents agrees that the asserted patents are directed to testing and debugging functionalities. And the specification makes clear that the normal system operation of the claimed integrated circuits may include test and debug operations. *See, e.g.*, Abstract ("Test

and debug circuits may be designed to observe states in user-definable circuits during the normal system operation of said user-definable circuits."); *see also* 14:11-33.

This claim phrase does not, however, specify a "mode" as that term is used in the specification, and the specification does not use "normal system operations" synonymously with normal mode or test mode. *See* 7:57-8:26. To the contrary, "[t]he specification . . . describes 'normal mode' and 'test mode' in the context of input and output signals, which terms do not define 'normal system operations.'" Ex. 11 [*Intellectual Ventures I LLC*, Dkt. 277] at 16. So it would not be appropriate to incorporate the additional limitations that Defendants propose.

E. "result data"

No.	Term	American's Proposed Construction	Defendants' Proposed Construction
5	result data (Claims 2, 8 of the '371 patent; Claims 5-7 of the '938 patent)	Plain and ordinary meaning *Alternatively:* data resulting from a testing process	data resulting from the execution of the instructions on the data received from the external [diagnostics] console

The parties primarily dispute whether this term requires construction at all. The words "result data" are understandable to a layperson and thus need no construction beyond their plain and ordinary meaning.

The patentee did not seek to redefine this term; in fact, the precise phrase "result data" does not appear in the specification. *See, e.g.*, *Nat'l Oilwell Varco, L.P. v. Auto-Dril, Inc.*, No. 5:09-cv-85, 2011 WL 3648532, at *12 (E.D. Tex. Aug. 16, 2011) (finding term "results" is "commonly understood and used consistently without definition" in patent specification, and should be given plain and ordinary meaning). Rather, the specification describes data resulting from testing processes in general terms consistent with the ordinary meaning of this phrase:

> Next, the diagnostics console 103 invoke[s] the IC 100 to execute its normal system operations. If and when the selected trigger event is detected and the analysis engine 215 has captured the required data, the diagnostics console 103 instructs the SPU 101 to transfer the captured data values out of the IC 100 and into the diagnostics console 103 where the data may be formatted and presented for analysis and interpretation.

14:20-27; *see also* 12:6-16, 12:35-40.

Although the specification generally describes a flow of information from the diagnostics console to the SPU and back out to the external diagnostics console, there is no need to construe "result data" in the overly narrow manner that Defendants propose. The claims themselves define this information flow. For example, claim 2 of the '371 patent recites:

> 2. The integrated circuit according to claim 1, further comprising at least one port selected from the group consisting of:
>
> a parallel I/O (PIO) port,
>
> a serial I/O (SIO) port, and
>
> a JTAG port;
>
> wherein data and instructions are to be sent through at least one of said ports to said service processor unit from an external diagnostics console, and wherein result data is to be sent through at least one of said ports from said service processor unit to said external diagnostics console.

15:11-22. To the extent Defendants' proposed construction is redundant of the existing claim language, it is superfluous. And to the extent it injects additional constraints and limitations that the patentee elected not to include in the claims, it is improper. *See Uniloc Luxembourg S.A. v. Compulink Bus. Sys., Inc.*, No. 2:11-cv-10122-MWF-PLA, 2013 WL 12123994, at *6 (C.D. Cal. Feb. 28, 2013) (construing term "result value" and noting that "tethering the term to its inclusion in a parameter is not required by the language of the claims, and the Court may not read a limitation from the specification into the claim terms").

In the alternative, if the Court determines that a construction is necessary for this claim phrase, the Court should construe it to mean "data resulting from a testing process." This is consistent with the plain and ordinary meaning of the term. *See, e.g.*, Ex. 6 [IBM Dict. of Computing] at 580 (defining "result": "An entity produced by the performance of an operation."); Ex. 5 [New Oxford Am. Dict.] at 1453 (defining "result": "an item of information obtained by experiment or some other scientific method[.]"); *see also* Ex. 7 [IEEE 100 The Authoritative Dict. of IEEE Stds. Terms] at 1166 (defining "test data:" "(1) Data from observations during tests."). American Patents' alternative construction accurately defines the

claim phrase, consistent with the specification and the claims, without importing repetitious or improperly limiting language.

F. "variable first-in, first-out (FIFO) element"

No.	Term	American's Proposed Construction	Defendants' Proposed Construction
6	variable first-in, first-out (FIFO) element (Claim 2 of the '716 patent; Claims 3, 16 of the '938 patent)	Plain and ordinary meaning	first-in, first-out (FIFO) element that delays the incoming signal by a programmable number of clock cycles

The parties dispute whether this term requires construction. Because the patents use this claim term in a manner consistent with its plain and ordinary meaning, the Court need not construe it.

The term first-in, first-out (or FIFO) has a plain and ordinary meaning to persons of ordinary skill in the art. *See, e.g.*, Ex. 7 [IEEE 100 The Authoritative Dict. of IEEE Stds. Terms] at 438 (defining "first-in, first-out": "Pertaining to a system in which the next item to exit the system is the item that has been in the system for the longest time."); Ex. 8 [Microsoft Comp. Dict.] at 215 (defining "first in, first out": "A method of processing a queue, in which items are removed in the same order in which they were added—the first in is the first out."); Ex. 6 [IBM Dict. of Computing] at 274 (defining "first-in-first-out (FIFO)": "A queuing technique in which the next item to be retrieved is the item that has been in the queue for the longest time.").

Defendants acknowledge that a FIFO element is a known term—indeed, their proposed construction retains this phrase, construing only the word "variable." But "variable" is also understandable to laypersons and describes something that can be varied or changed. *See, e.g.*, Ex. 5 [New Oxford Am. Dict.] at 1870 (defining "variable" as "able to be changed or adapted").

Thus, a person having ordinary skill in the art would understand the phase "variable FIFO element" to mean a FIFO element that can be varied or changed. In an embodiment, the

specification describes that this may be accomplished by having a variable shift depth which controls the number of register stages which are bypassed:

> Fig. 9b shows the circuit details of each variable First-In-First-Out shift register (FIFO) 804, each having a number of serially-connected register stages 812. Each register stage 812 has a multiplexer which, under control of a decoder 811, selects between the signal held in a flip-flop of that stage or the incoming signal to the stage to place on the stage's output terminal. The shift depth of each variable FIFO 804 is programmable by the SPU 101 by setting a count register 810 for each bit feeding the analysis engine 215. The value in the count register 810 is decoded by the decoder 811. The result controls the number of register stages 812 which are bypassed. This compensates for the path delay differences among the different probe points by realigning capture times of signals captured in the analysis engine 215.

10:50-63; *see also* Figs. 9a & 9b. The specification's description of the variable FIFO elements is consistent with the plain and ordinary meaning of this claim phrase.

By contrast, Defendants' implicit construction of "variable"—something "that delays the incoming signal by a programmable number of clock cycles"—is overly narrow and is not found in the specification. Given that it ladles in added technical verbiage while not construing the core portion of the term—first-in, first-out (FIFO) element—Defendants' construction makes the disputed phrase more difficult for a jury to understand, not less.

VI. DISPUTED CLAIM TERMS (MEANS-PLUS-FUNCTION)

A. Construction of Means-Plus-Function Claims

When it applies, § 112, ¶ 6 limits the scope of the functional term "to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347 (Fed. Cir. 2015) (en banc in relevant portion). Construing a means-plus-function limitation involves multiple steps. "The first step … is a determination of the function of the means-plus function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). "[T]he next step is to determine the corresponding structure disclosed in the

specification and equivalents thereof." *Id*. A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id*.

"While corresponding structure need not include all things necessary to enable the claimed invention to work, it must include all structure that actually performs the recited function." *Telcordia Techs., Inc. v. Cisco Sys., Inc.*, 612 F.3d 1365, 1376 (Fed. Cir. 2010). As such, "[w]hen multiple embodiments in the specification correspond to the claimed function, proper application of § 112 ¶ 6 generally reads the claim element to embrace each of those embodiments . . . ." *Micro Chem., Inc. v. Great Plains Chem. Co., Inc.*, 194 F.3d 1250, 1258-59 (Fed. Cir. 1999); *see also Creo Prods., Inc. v. Presstek, Inc.*, 305 F.3d 1337, 1346 (Fed. Cir. 2002) (holding that proper application of § 112 ¶ 6 "generally reads the claim element to embrace distinct and alternative described structures for performing the claimed function"). But § 112 ¶ 6 does not permit "incorporation of structure from the written description beyond that necessary to perform the claimed function." *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

B. "means to capture said signals from said probe lines"

No.	Disputed Term	American's Proposed Construction	Defendants' Proposed Construction
7	means to capture said signals from said probe lines (Claim 5 of the '001 Patent)	Function: capture said signals from said probe lines Structure: input terminals of analysis engine 215 (as shown in Fig. 9a) or channels of the logic analyzer 215 (as shown in Fig. 11), and equivalents thereof	Function: capture said signals from said probe lines; Structure: channels of the logic analyzer 215, as shown in Fig. 11. Alternatively, if this means-plus-function term is not limited to being an element of the "input ports of said on-chip logic analyzer," the corresponding structure is plurality of flip-flops 805

			in conjunction with a digital phase locked loop (PLL) 802 having selectable clock outputs 803 to each flip-flop 805 to tune when the data from each probe point is to be captured, as shown in Fig. 9a, and equivalents thereof.

The parties agree that this is a means-plus-function limitation. The parties also agree that the function for this limitation is "capture said signals from said probe lines." The parties dispute, however, what structure corresponds to the agreed function.

The Court should adopt American Patents' proposed structure (input terminals of analysis engine 215 (as shown in Fig. 9a) or channels of the logic analyzer 215 (as shown in Fig. 11), and equivalents thereof) because those two structures are described by the specification as performing the claimed function of "captur[ing] said signals from said probe lines." First, as Defendants admit via their proposed construction, "channels of the logic analyzer, as shown in Fig. 11" is structure that performs the claimed function. Indeed, the specification clearly links the channels of the logic analyzer to the claimed function of capturing signals from said probe lines: "The selections are achieved by coupling the signals for digital probes 202 to the channels of the analysis engine 215 … to allow ***the signals on the digital probes 202 value to be captured onto channels of the logic analyzer***." *See* 12:46-51; *see also* 12:43-45, 51-56 and 14:6-10 (emphasis added).

Likewise, "input terminals of analysis engine 215, as shown in Fig. 9a" are structure that performs the claimed function. Fig. 9a shows the inputs and input terminals of analysis engine 215. *See* Fig. 9a; 4:10-11 (describing Fig. 9a as "a block diagram of an input aligner portion of Analysis Engine of the FIG. 2 SPU"). The specification links that structure shown in Fig. 9a to the claimed function of capturing signals from said probe lines: "FIG. 9a shows an embodiment of the analysis engine 215 which, under the control of the microprocessor 211, ***captures logic signals from the test bus***." 10:23-25; *see also* 10:37-42, 10:64-65 (emphasis added).

Defendants appear to assert that one of the structures identified above (input terminals of analysis engine 215 (as shown in Fig. 9a))[2] is not part of the "input ports" of said on-chip logic analyzer. That argument makes little sense. Fig. 9a itself has labels showing "Scan & Probe Inputs," and Fig. 9a is described as showing the "input aligner portion" of analysis engine 215. *See* 4:10-12; Fig. 9a. The input aligner portion, which has "Scan & Probe Inputs," is certainly part of the input ports.

The parties appear to agree that at least "channels of the logic analyzer 215 (as shown in Fig. 11)" constitute corresponding structure for the "capture said signals from said probe lines" function. Defendants' alternate construction (plurality of flip-flops 805 in conjunction with a digital phase locked loop (PLL) 802 having selectable clock outputs 803 to each flip-flop 805 to tune when the data from each probe point is to be captured, as shown in Fig. 9a) should be rejected because it incorporates structure "beyond that necessary to perform the claimed function." *See Micro Chem.*, 194 F.3d at 1258; *see also Safegate Airport Sys., Inc. v. RLG Docking Sys., Inc.*, No. CV-13-567-PHX-GMS, 2014 WL 3397774, at *5 (D. Ariz. Jul. 11, 2014) (construing "means for projecting" as "a mirror" instead of "using 2 mirrors (one for horizontal scan, one for vertical scan), each mirror separately controlled by a step motor" where specification disclosed using two mirrors, each controlled by a step motor, because "the specification does not contain limiting language that states that two mirrors must be used[.]"). In particular, the digital phase locked loop (PLL) 802 and its selectable clock outputs 803 are not necessary to perform the function of "captur[ing] said signals from said probe lines." Instead, those structures are one way to trigger flip flops 805 to capture signals. But that does not mean PLL 802 and selectable clock outputs 803 capture signals themselves.

[2] Defendants admit that the other structure (channels of the logic analyzer 215 (as shown in Fig. 11)) are input ports of said on-chip logic analyzer, and for good reason. The channels are plainly described as where signals on the digital probes are captured. *See* 12:46-51.

C. "means to align said signals propagated through said probe lines to create aligned signals"

No.	Disputed Term	American's Proposed Construction	Defendants' Proposed Construction
8	means to align said signals propagated through said probe lines to create aligned signals (Claim 5 of the '001 Patent)	Function: align said signals propagated through said probe lines to create aligned signals Structure: input aligner portion of analysis engine 215 (as shown in Fig. 9a) or probe storage elements 1000 (as shown in Fig. 11), and equivalents thereof	Function: align said signals propagated through said probe lines to create aligned signals; Structure: no corresponding structure. Alternatively, if this means-plus-function term is not limited to being an element of the "input ports of said on-chip logic analyzer," the corresponding structure is the variable FIFO shift registers 804, as shown in Figs. 9a and 9b, and equivalents thereof.

The parties agree this is a means-plus-function limitation and that the function for this limitation is "align said signals propagated through said probe lines to create aligned signals." The parties dispute, however, whether the specification discloses corresponding structure for the agreed function and, if so, what that structure is.

For this and the remaining means-plus-function terms, Defendants admit that the specification discloses structures that carry out the claimed functions. But Defendants apparently believe that the patentee somehow drafted claims that were too narrow to cover the very structures that it disclosed for performing the claimed functions. And Defendants apparently believe that they can make this showing by clear and convincing evidence, as they must do in order to invalidate these claims for indefiniteness. Defendants' position is contrary not only to both bedrock claim construction principles, but also to common sense.

The Court should adopt Plaintiff's proposed structure (input aligner portion of analysis engine 215 (as shown in Fig. 9a) or probe storage elements 1000 (as shown in Fig. 11), and

equivalents thereof) because those structures are described by the specification as performing the claimed function of "align[ing] said signals propagated through said probe lines to create aligned signals." First, the specification clearly links the "input aligner portion of analysis engine 215 (as shown in Fig. 9a)" to performance of the claimed function. For example, Fig. 9a is described as "a block diagram of an input ***aligner*** portion of Analysis Engine of the FIG. 2 SPU," and Fig. 9b is described as "a detail of the FIG. 9a Analysis Engine's input ***aligner***." *See* 4:10-12 (emphasis added). The specification further clearly links this structure to the claimed function by describing how the variable FIFO shift registers shown in Figs. 9a and 9b align captured signals: "The shift depth of each variable FIFO 804 is programmable by the SPU 101 by setting a count register 810 for each bit feeding the analysis engine 215. The value in the count register 810 is decoded by the decoder 811. The result controls the number of register stages 812 which are bypassed. This ***compensates for the path delay differences*** among the different probe points by ***realigning capture times of signals captured*** in the analysis engine 215." *See* 10:56-64 (emphasis added).

Likewise, the specification clearly links "probe storage elements 1000, as shown in Fig. 11" to the claimed function of "align[ing] said signals propagated through said probe lines to create aligned signals." The specification first links probe storage elements 1000 to the claimed function by describing how clocking of the probe storage elements 1000 ensure that all signals are aligned (through ensuring that their "cycle relationship to one another is preserved"): "Each channel of the analysis engine 215 contains zero or more number of PSEs 1000 which are clocked by a common periodic clock signal labeled 'Cf' on a clock signal line 1001…. This way all signals captured on the analysis engine 215 channels arrive at the end of the channels after a fixed, predetermined number of clock cycles so that their cycle relationship to one another is preserved, regardless of the length (i.e., number of bits) of the individual channels of analysis engine 215." *See* 12:51-67 (emphasis added). The specification also links probe storage elements 1000 to the claimed function by describing how the number of PSEs 1000 on each

channel can be used by software processes in an outside system "to ***align the data*** with respect to one another." *See* 13:1-4 (emphasis added).

Although Defendants admit that there is structure disclosed that carries out the claimed function—"align said signals propagated through said probe lines to create aligned signals"—Defendants assert that there is no corresponding structure that is part of the "input ports" of said on-chip logic analyzer. Defendants appear to attribute a very narrow meaning to "input ports"—so narrow as to only include input terminals.

The term "input ports" should not be so limited. For example, "The Authoritative Dictionary of IEEE Standards Terms" (7th Ed.) defines "input" as "Pertaining to a device, process, or channel involved in the reception of data." Ex. 7 at 556-57. Likewise, the court in *Personalized Media Communications, LLC v. Apple, Inc.*, No. 2:15-cv-1366-JRG-RSP, 2016 WL 6247054 (E.D. Tex. Oct. 25, 2016), gave the term "input ports" a similarly broad definition: "structure for receiving signals into a device." *See id.* at *25. The structure of claim 5 also suggests a broader definition for "input ports" by requiring that the claimed "input ports" have at least three functions: (1) capturing signals from probe lines; (2) aligning signals to create aligned signals; and (3) capturing aligned signals. So to the extent that there is any doubt whether a broader or narrower meaning of input ports is appropriate, the claim structure supports a reading broad enough to include the structures of the on-chip logic analyzer that perform these functions.

An appropriately broad definition of "input ports" would encompass what is shown in Fig. 9a (described as "a block diagram of an input aligner portion of Analysis Engine of the FIG. 2 SPU") as well as what is shown in Fig. 11 (described as showing "a probe string connection of probe points to the buffer memory using logic analyzer channels that are implemented with probe storage elements (PSE)"). The structures shown in those figures allow for the receipt and processing of input to the on-chip logic analyzer, as suggested by the structure of claim 5.

Both of the structures identified by Plaintiff are part of the "input ports." For example, "probe storage elements 1000" are part of the input ports. The specification notes that probe

storage elements 1000 "form[]" the channels of logic analyzer 215. *See* 12:51-52. And as noted above, Defendants concede that the channels of the logic analyzer 215 are part of the input ports.

The "input aligner portion of analysis engine 215 (as shown in Fig. 9a)" is also part of the input ports of said on-chip logic analyzer. Fig. 9a is described as showing the "input aligner portion" of analysis engine 215, and the figure itself has labels showing "Scan & Probe Inputs." *See* 4:10-12; Fig. 9a. The input aligner portion, which has "Scan & Probe Inputs," is plainly part of the input ports.

Defendants' alternate construction (variable FIFO shift registers 804, as shown in Figs. 9a and 9b) should be rejected because it fails to incorporate "all structure that actually performs the recited function." *Telcordia,* 612 F.3d at 1376. In particular, the detail of variable FIFO 804 that is shown in Fig. 9b is simply a component of the input aligner portion of the analysis engine. It is that larger structure that the specification clearly links to the claimed function.

The Court should also reject Defendants' alternate construction because it ignores Fig. 11, which shows a "distinct and alternative" way of aligning signals as compared with Fig. 9a. *See Creo*, 305 F.3d at 1346.

D. "means to capture said aligned signals"

No.	Disputed Term	American's Proposed Construction	Defendants' Proposed Construction
9	means to capture said aligned signals (Claim 5 of the '001 Patent)	Function: capture said aligned signals Structure: Variable FIFO 804 (as shown in Fig. 9a), probe storage elements 1000 or buffer memory 218 (as shown in Fig. 11), and equivalents thereof	Function: capture said aligned signals; Structure: no corresponding structure. Alternatively, if this means-plus-function term is not limited to being an element of the "input ports of said on-chip logic analyzer," the corresponding structure is the output from the variable FIFO shift registers 804 (such output labeled 814 in Figs. 9a/9c, which is also

			an input to buffer memory 218), and equivalents thereof.

The parties agree this is a means-plus-function limitation. The parties also agree that the function for this limitation is "capture said aligned signals." The parties dispute, however, whether the specification discloses corresponding structure for the agreed function and, if so, what that structure is.

The Court should adopt Plaintiff's proposed structure (Variable FIFO 804 (as shown in Fig. 9a), probe storage elements 1000 or buffer memory 218 (as shown in Fig. 11), and equivalents thereof) because those structures are described by the specification as performing the claimed function of "captur[ing] said aligned signals."

First, Defendants admit, through their alternate proposed structure ("the output from the variable FIFO shift registers 804 (such output labeled 814 in Figs. 9a/9c, which is also an input to buffer memory 218)"), that Variable FIFO 804 (as shown in Fig. 9a) plays a role in performing the function of "captur[ing] said aligned signals." Indeed, the specification clearly links variable FIFO 804 to the claimed function by describing how "the analysis engine 215 ***collects data*** into the buffer memory ***from the variable FIFOs 804***[.]" *See* 11:21-23 (emphasis added). Data could not be "collected from" the variable FIFO 804 if the variable FIFO 804 had not ***captured*** that data. And the "data" in variable FIFO 804 that is referred to includes aligned signals, as the specification describes how features of the variable FIFOs 804 allow for "***compensat[ion] for the path delay differences*** among the different probe points by realigning capture times of signals captured in the analysis engine 215." *See* 10:61-63 (emphasis added).

Probe storage elements 1000 (as shown in Fig. 11) are also structure that performs the claimed function. The specification clearly links probe storage elements 1000 to the function of "captur[ing] said aligned signals" by describing them as forming "a distributed serial shift register," a device that necessarily captures signals. *See* 12:51-54. Those signals that are captured are aligned: "all signals captured on the analysis engine 215 channels arrive at the end

of the channels after a fixed, predetermined number of clock cycles so that ***their cycle relationship to one another is preserved***[.]" *See* 12:62-65 (emphasis added).

Likewise, buffer memory 218 (as shown in Fig. 11) is structure that performs the claimed function. The specification clearly links buffer memory 218 to the function of capturing said aligned signals: "Once enabled, the analysis engine 215 ***captures new values first*** into the flip-flops along the OLA channels and ***subsequently into the buffer memory 218***[.]" *See* 14:6-10; *see also* 12:51-56 (emphasis added). Because the signals were aligned coming out of the probe storage elements 1000, the values captured by buffer memory 218 are aligned signals.

Although Defendants admit that there is structure disclosed that performs the claimed function—"capture said aligned signals"—Defendants again assert that there is no corresponding structure that is part of the "input ports" of said on-chip logic analyzer. But all three of the structures identified by American Patents are part of the "input ports."

For example, as explained above, "probe storage elements 1000" are part of the input ports. Likewise, variable FIFO 804 is part of the input ports. Figures 9a and 9b both show variable FIFOs 804, and the specification describes those figures as "a block diagram of an input aligner portion of Analysis Engine of the FIG. 2 SPU" and "a detail of the FIG. 9a Analysis Engine's input aligner" respectively. Because variable FIFOs 804 are a part of the input aligner, they are also part of the input ports.

Buffer memory 218 (as shown in Fig. 11) is also part of the input ports. The specification describes how data are moved "towards the ***end of the logic analyzer channel*** where the data are stored in buffer memory 218." 12:51-56. So just like probe storage elements 1000, buffer memory 218 is also part of the logic analyzer channel, which Defendants have admitted are part of the input ports of the OLA.

The Court should reject Defendants' alternate construction (the output from the variable FIFO shift registers 804 (such output labeled 814 in Figs. 9a/9c), which is also an input to buffer memory 218) because it incorporates structure "beyond that necessary to perform the claimed function." *See Micro Chem.*, 194 F.3d at 1258. In particular, as explained above, variable FIFO

804 captures aligned signals. Defendants include the ***output*** of variable FIFO 804, which may be aligned signals, but which is not structure that ***captures*** aligned signals.

Defendants' alternate construction should also be rejected because it ignores Fig. 11, which shows two additional "distinct and alternative" ways of capturing aligned signals as compared to Fig. 9a. *See Creo*, 305 F.3d at 1346.

E. "means to transfer said aligned signals out of said integrated circuit"

No.	Disputed Term	American's Proposed Construction	Defendants' Proposed Construction
10	means to transfer said aligned signals out of said integrated circuit (Claim 6 of the '001 Patent)	Function: transfer said aligned signals out of said integrated circuit Structure: TAP 217, SIO interface 210, PIO interface 216, or scan data output terminal SO, and equivalents thereof	Function: transfer said aligned signals out of said integrated circuit; Structure: no corresponding structure. Alternatively, if this means-plus-function term is not limited to being an element of the "on-chip logic analyzer," the corresponding structure is the TAP interface 217 and the SIO interface 210, as shown in Fig. 2, and equivalents thereof.

The parties agree that this is a means-plus-function limitation. The parties also agree that the function for this limitation is "transfer said aligned signals out of said integrated circuit." The parties dispute, however, whether the specification discloses corresponding structure for the agreed function and, if so, what that structure is.

The Court should adopt American Patents' proposed structure (TAP 217, SIO interface 210, PIO interface 216, or scan data output terminal SO, and equivalents thereof) because those four structures are clearly linked in the specification to the claimed function of "transfer[ring] said aligned signals out of said integrated circuit."

First, the specification clearly links each of TAP 217, SIO interface 210, and PIO interface 216 with performing the function of "transfer[ring] said aligned signals out of said integrated circuit." For example, the specification provides: "To provide ***communication between the external world and the SPU 101***, the bus 219 is also connected to a serial input/output (SIO) interface 210, a parallel input/output interface (PIO) 216, and a test access port (TAP) 217." *See* 6:41-49 (emphasis added). The specification also states that analysis engine 215 is "where [the selected probe signal] is captured ***for subsequent off-line analysis***," meaning that the aligned signals stored with the analysis engine are sent outside of the integrated circuit. *See* 10:40-42 (emphasis added).

Scan data output terminal SO is also structure that performs the claimed function. The specification clearly links scan data output terminal SO to the claimed function: "[t]he ***output terminal*** of the latch 1107 forms a ***scan data output terminal***, SO, and is also connected to the control terminal of the multiplexer 1108." *See* 13:40-42. The specification also refers to what happens "after the captured data has been transported to the external diagnostics console," confirming that the captured data is sent outside of the integrated circuit. *See* 13:1-4 (emphasis added). This makes sense, as the scan output of the last element in a chain of scannable latches is ultimately how information is fed out of the chain.

Although Defendants again admit that there is structure disclosed that carries out the claimed function— transfer said aligned signals out of said integrated circuit—Defendants assert that there is no corresponding structure that is an element of said on-chip logic analyzer. But all four of the structures identified by Plaintiff are elements of said on-chip logic analyzer. For example, each of TAP 217, SIO interface 210, and PIO interface 216 are shown in Fig. 2 as being connected to analysis engine 215 via processor bus 219. Likewise, scan data output terminal SO is an element of logic analyzer 215. Scan data output terminal SO is an element of PSE 1000, *see* 13:25-42; Fig. 13, and as explained above, PSE 1000 is part of on-chip logic analyzer 215.

Defendants' alternate construction (the TAP interface 217 and the SIO interface 210, as shown in Fig. 2) should be rejected because it ignores PIO interface 216 and scan data output terminal SO, which are additional "distinct and alternative" ways of transferring aligned signals as compared to Fig. 9a. *See Creo*, 305 F.3d at 1346.

VII. CONCLUSION

For the foregoing reasons, the Court should adopt American Patents' proposed claim constructions and reject Defendants' proposed claim constructions.

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Respectfully submitted,

/s/ Larry D. Thompson, Jr.
Matthew J. Antonelli (*admission pending*)
Texas Bar No. 24068432
matt@ahtlawfirm.com
Zachariah S. Harrington (lead attorney)
Texas Bar No. 24057886
zac@ahtlawfirm.com
Larry D. Thompson, Jr.
Texas Bar No. 24051428
larry@ahtlawfirm.com
Christopher Ryan Pinckney (*admission pending*)
Texas Bar No. 24067819
ryan@ahtlawfirm.com
Michael D. Ellis
Texas Bar No. 24081586
michael@ahtlawfirm.com

ANTONELLI, HARRINGTON
& THOMPSON LLP
4306 Yoakum Blvd., Ste. 450
Houston, TX 77006
(713) 581-3000

Stafford Davis
State Bar No. 24054605
sdavis@stafforddavisfirm.com
Catherine Bartles
Texas Bar No. 24104849
cbartles@stafforddavisfirm.com
THE STAFFORD DAVIS FIRM

The People's Petroleum Building
102 North College Avenue, 13th Floor
Tyler, Texas 75702
(903) 593-7000
(903) 705-7369 fax

Attorneys for American Patents LLC